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EXAMINER	
ZERVIGON, RUDY	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/829,587
Filing Date: April 09, 2001
Appellant(s): LAPTEV, PAVEL N.

Sheldon R. Meyer
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 26, 2006 appealing from the Office action mailed July 11, 2003.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

(9) Grounds of Rejection

The following grounds of rejection are applicable to the appealed claims:

Claims 1-4, 7-9, 11, 14-16, 19-21, 43, 44, 45, 46, 47, and 50 are rejected under 35 U.S.C. 102(b) as being anticipated by Koshimizu (USPat. 5,980,687) and demonstrated by Mountsier et al (USPat. 5,810,933)[1].

Claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49, and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koshimizu (USPat. 5,980,687) in view of Mountsier et al (USPat. 5,810,933).

Claims 1-21, and 43-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's own admitted prior art in view of Mountsier et al (USPat. 5,810,933).

(10) Response to Argument

Applicant states:

"

Applicant submits that the invention disclosed in the present application is the separation of the electrodes and the wafer, which provides a smoother surface on the wafer after etching.

"

In regards to the claimed invention of the present application, the Examiner's position concerning the claimed "spacing" of the electrodes and the wafer is an invention feature that is overwhelmingly anticipated in the prior art as is demonstrated by Mountsier et al (USPat. 5,810,933). The teachings of Mountsier's Figures 5 and 6 as conveyed in the Examiner's Final Rejection define Applicant's invention of the claimed "spacing" of the electrodes and the wafer. Once appreciated, Mountsier's Figures 5 and 6 demonstrate that "spacing" exists between wafers and surfaces supporting them including electrode surfaces. Absent the claimed "spacing" feature, Applicant's structural features of the claimed invention

are clearly conveyed in an element-by-element correspondance to Koshimizu (USPat. 5,980,687) as described by the Examiner's final rejection. The Examiner's addition of Mountsier is only a demonstration of the inherency in any structure that supports a wafer (wafer support, platen, electrostatic chuck, table, stage, electrode, as is known in the art) – Applicant's claimed "spacing" of the electrode(s) and the wafer is an inherent attribute of Koshimizu as demonstrated by Mountsier.

Applicant further states "Further, Koshimizu also discloses that the wafer W is fixed on the surface of either electrode 110 or 116" with subsequent quotations from Koshimizu in support thereof. In response, the Examiner notes that Koshimizu's "fixation" of the wafer, or lack thereof, is not in any means a limiting feature in Koshimizu when teaching Applicant's invention of the claimed "spacing" of the electrodes and the wafer. Koshimizu's "fixation" is identical to applicant's claimed "spacing" as demonstrated by Mountsier.

Applicant states:

"

Applicant submits that "have a gap" is different from "separation". "Separation between a wafer and a support" means that the wafer and the support do not contact at a point. In other words, "separation" means there is no contacting point at all at the wafer-support interface. Generally speaking, separation between two articles implies a complete separation between these two articles. "Have a gap" means that there exists some local separations, meaning that there are some locations at the wafer-support interface where the wafer surface and the support surface are separated. Thus it is possible for a wafer and a support to have a gap between them but they are not separated. In other words, A and B are separated also means that A and B have a gap between them. But the reverse is not necessarily true. A and B have a gap

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[1] MPEP 2121.01

between them does not necessarily means that A and B are separated....Thus applicant agrees with the Examiner that there is always a gap (at least in the microscopic scale) between the wafer and the support, but respectfully submits that this does not indicate nor imply that the wafer and the support are separated as disclosed in the present application.

" (pages 9-10, Final Brief)

In response, the Examiner emphasizes that the claimed invention does not specify the word "separation" in any of the finally rejected claims. Applicant does claim a "spaced" relationship between the wafer and an electrode surface. As a result, Applicant's above-quoted arguments do not address the Examiner's rejections of the claimed invention.

Subsequently, Applicant states:

"

Applicant submits that the claim language of "spaced from", together with the specification language of "separation", means that the wafer is spaced from the two electrodes, that the wafer is separated from the two electrodes, and that the wafer does not possess any contact point with the two electrodes.

" (Pages 11-12, Reference to claims 1, 7, 8, and 11 Final Brief)

In response, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. (See MPEP § 2145, § 2111 - § 2116.01; In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1571-72, 7 USPQ2d 1057, 1064-1065 (Fed. Cir.), cert. denied, 488 U.S. 892 (1988); Ex parte McCullough, 7 USPQ2d 1889, 1891 (Bd. Pat. App. & Inter. 1987).

With respect to Applicant's claim 14 argument:

"

Claim 14: Claim 14 provides: "... the second electrode and the wafer providing a first capacitor ..." Applicant submits that for the second electrode and the wafer to form a capacitor, they have to be separated, not just having a gap, since any contact point would electrically connect the electrode and the wafer, and thus forming a conductor, not a capacitor.

"

In response, because the Mountsier et al (USPat. 5,810,933) patent demonstrates the established knowledge in the art of gap(s) and spacing(s) between the wafer and its support surface, claimed features of the claimed apparatus are presumed to proove inherency. When the structure recited in the references is substantially identical to that of the claims, claimed properties or functions are presumed to be inherent. Where the claimed and prior art products are identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a prima facie case of either anticipation or obviousness has been established. In re Best, 562 F.2d 1252, 1255, 195 USPQ 430, 433 (CCPA1977). Further, regarding electrical continuity as proof or disproof for establishing capacitance, the Examiner argues that charge separation (i.e. capacitance) is generated between gaps of dissimilar materials each of which have dissimilar conductivity (see Mountsier for materials – column 5; lines 10-15). In particular, it is both necessary and required for Mountsier's apparatus to establish and maintain a capacitance between Mountsier's wafer (62, Figure 5,6) and Mountsier's ceramic disk (52, Figure 5,6) for Mountsier's wafer to be mounted "..to the WCD using electrostatic force by methods well known to those skilled in the art." (column 5, lines 10-13). For an "electrostatic force" to be used to hold a wafer and its support at an interface, a charge separation, or capacitance must be established per Coulomb's law and its related force equation.

With respect to claim 20, Applicant states:

“

“... the wafer having a floating potential ...” Applicant submits that for the wafer to have a floating potential, the wafer has to be separated from both electrodes, since a contact with an electrode will provide the wafer with the potential of that electrode.

“

In response, the Examiner disagress that “a contact with an electrode will provide the wafer with the potential of that electrode” resulting in a loss of the “floating” state – a floating state implies an intended use of the claimed apparatus components. The Examiner argues that Mountsier was cited as teaching apparatus capable of performing the intended use. In particular, Mountsier was cited as teaching a wafer support platform (52, Figure 5; column 4, lines 20-23) that provides a series relationship between two capacitors, one (68 dielectric gap; Figure 5; column 4, lines 2023) having a high capacity impedance and the other (80/82 dielectric gap; Figure 6) having a low capacity impedance. In particular, because the wafer support 52 is made of an electrical insulator (ceramic, column 5, lines 8-20) capacitance across the stated points is established and the wafer (62) is electrically floated. Indeed, the Examiner’s approach in assessing the teaching in the prior art was to consider how applicant’s claimed invention establishes the floating state of the electrode. The first half of claim 20 establishes how the floating potential can be attained:

“

a first electrically conductive member disposed in adjacent but spaced relationship to the first electrode and having a reference potential to provide an electrical field between the first electrode and the first electrically conductive member,

a second electrically conductive member disposed in adjacent but spaced relationship to the second electrode and having the reference potential to provide an electrical field between the second electrode and the second electrically conductive member,

the wafer having a floating potential...

"

In the context of the above claimed features, Koshimizu was cited in the final rejection (page 14) as teaching a first electrically conductive member (104, Figure 1,3) disposed adjacent the first electrode (116, Figure 1,3) for providing a reference potential different in magnitude (grounded, see Figure 1,3) from the bias on the first electrode (116, Figure 1,3) to create a first electrical field, and a second electrically conductive member (204, Figure 3, 4) disposed adjacent the second electrode (110, Figure 1,3) for providing the reference potential (also grounded - 204/208 contact with grounded 104 via 106 and 208/104 contact; Figures 3, 4) to create a second electrical field between the second electrode (110, Figure 1,3) and the second electrically conductive member (204, Figure 3, 4).

The Examiner then stated in his final rejection that because Mountsier teaches the wafer support 52 is made of an electrical insulator (ceramic, column 5, lines 8-20) capacitance across the stated points is established and the wafer (62) is electrically floated. This is the same physical organization as Applicant's invention (Figure 2), however, it is noted that Figure 2 is a description of the wafer and not the supporting apparatus of which the pending claims describe. The only reference to any structure providing a floating potential to the wafer in Applicant's invention as originally filed is: "The wafer 16 is at a floating potential." (Page 8, lines 18-19).

Applicant states:

"

Applicant submits that the language of "displaced from each other" and "displaced from the wafer", together with the specification language of "separation", means that the wafer is displaced from the two electrodes, that the wafer is separated from the two electrodes, and that the wafer does not possess any contact point with the two electrodes.

" (page 13, Final Brief)

and...

"

To have a construction of two capacitors in series, there needs to be three electrodes (electrode 1, electrode 2, and electrode 3) and two insulators (insulator 1, and insulator 2) with the insulator 1 disposed between electrodes 1 and 2, and the insulator 2 disposed between electrodes 2 and 3.

" (page 14, Final Brief)

As previously stated, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. (See MPEP § 2145, § 2111 - § 2116.01; In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 1571-72, 7 USPQ2d 1057, 1064-1065 (Fed. Cir.), cert. denied, 488 U.S. 892 (1988); Ex parte McCullough, 7 USPQ2d 1889, 1891 (Bd. Pat. App. & Inter. 1987). The Examiner remphasizes that the claimed invention does not specify the word "separation" in any of the finally rejected claims. Applicant does claim a relationship between the wafer and an electrode surface as being "spaced", "displaced from each other", and "displaced from the wafer". Nor does applicant claim the above-stated collection of electrodes and insulators which are substrate features and not apparatus features in the pending apparatus claims. The teachings of Mountsier's Figures 5 and 6 as conveyed in the Examiner's Final Rejection define Applicant's invention of the claimed "spacing", "displaced from each other", and "displaced from the wafer" between the electrode and the wafer. Once appreciated, Mountsier's Figures 5 and 6 demonstrate that "spacing" and "displacement" exist between wafers and surfaces supporting them including electrode surfaces.

With respect to the Examiner's rejection of claims 5, 6, 10, 12, 13, 17, 18, 20, 48, 49 and 51 under 35 U.S.C. 103(a) as being unpatentable over Koshimizu (5,980,687) in view of Mountsier et al. (5,810,933), applicant states:

"

There is no motivation nor suggestion for Koshimizu to replace his wafer support platform with Mountsier et al.'s wafer support platform.

"

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, there is teaching, suggestion, and motivation for the combination of Koshimizu (5,980,687) in view of Mountsier et al. (5,810,933). In particular, Mountsier's patent is wholly directed to favorable reasons to effect the Examiner's proposed "alternate means for supporting the substrate". In particular, the Examiner's "alternate means" references Mountsier's benefits for his "WCD" which the Examiner recites in the rejection as wafer support platform (52, Figure 5; column 4, lines 20-23). Indeed, Mountsier's universal motivation for his WCD is for uniform substrate temperature control (column 2, lines 5-10) to meet various process criteria established by manufacturers (column 2, lines 1-2).

Applicant's discussions and Figure on page 15 of the final brief appears to present arguments centered on the attributes of the processed wafer, and not on the claimed apparatus components. The wafer, and it's

attributes, are not structural features weighed in the pending appratus claims. Further, it has been established that apparatus claims must be structurally distinguishable from the prior art (In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ2d 1429, 1431-32 (Fed. Cir. 1997) MPEP 2114). Moreover, it is well established that the material or article worked upon i.e. (wafer) does not limit apparatus claims – MPEP 2115 (Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969); In re Young, 75 F.2d 966, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 312 F.2d 937, 136 USPQ 458, 459 (CCPA 1963)); In In re Casey, 370 F.2d 576, 152 USPQ 235 (CCPA 1967).

(11) Related Proceeding(s) Appendix

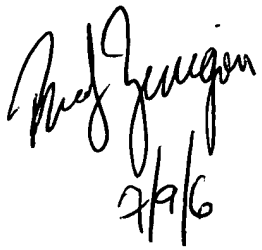
No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Rudy Zervigon

Primary Examiner, Art Unit 1763



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